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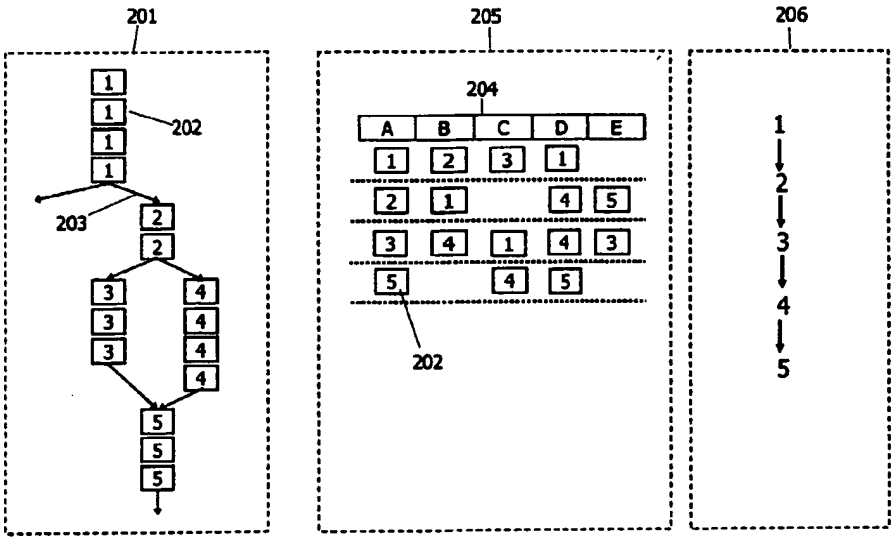
(54) Title: MICROPROCESSOR INSTRUCTION EXECUTION METHOD FOR EXPLOITING PARALLELISM



(57) Abstract: A low overhead mechanism for supporting speculative execution and code compression in a Very Long Instruction Word (VLIW) microprocessor. Profitable speculations can be determined statically at compile time and a low overhead hardware recovery mechanism used that does not require compensation code.

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